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1 [Scheduling designs into a time-multiplexed FPGA](#)



Steve Trimberger

 March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

Publisher: ACM Press

 Full text available: [pdf\(797.35 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

An algorithm is presented for partitioning a design in time. The algorithm divides a large, technology-mapped design into multiple configurations of a time-multiplexed FPGA. These configurations are rapidly executed in the FPGA to emulate the large design. The tool includes facilities for optimizing the partitioning to improve routability, for fitting the design into more configurations than the depth of the critical path and for compressing the critical path of the design into fewer config ...

2 [Buffer minimization and time-multiplexed I/O on dynamically reconfigurable FPGAs](#)



Douglas Chang, Malgorzata Marek-Sadowska

 February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

 Full text available: [pdf\(1.10 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Network flow based circuit partitioning for time-multiplexed FPGAs](#)



Huiqun Liu, D. F. Wong

 November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

 Full text available: [pdf\(957.50 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

4 [A graph theoretic optimal algorithm for schedule compression in time-multiplexed FPGA partitioning](#)

Huiqun Liu, D. F. Wong

 November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**